REMARKS

Claims 1-14, 25-31, and 41-71 stand rejected in the present application. Claims 1-8 and 41-71 have been cancelled. Claims 9, 13, 25, and 31 have been amended. New claims 72-77 have been added. Claims 9-14, 25-31, and 72-77 are pending in the application. Applicant requests reconsideration of these pending claims.

Applicant has amended the title to correct errors of a typographical nature. This amendment is reflected in the Amendment to the Specification.

Claims 9-14 and 25-31 stand rejected as either anticipated by, or obvious in view of, U.S. Patent 5,882,994 to Araki, et al. ("Araki"). Applicant requests reconsideration of such rejections.

Claim 9 has been amended and as amended recites a method of forming a floating gate transistor that includes, in pertinent part, forming an oxide layer over a semiconductive substrate and forming a first layer of conductively doped semiconductive material upon the oxide layer, the first layer of conductively doped semiconductive material contacting the oxide layer. Claim 9 further recites forming a second layer of substantially undoped semiconductive material over the first layer.

For a reference to anticipate this or any other claim, the reference must teach every element of the claim. (MPEP §2131, 8th ed.) Furthermore, to establish a prima fascia case of obviousness, the references must teach or suggest all elements of the claimed invention. (MPEP §706.02(j)). The cited reference does not teach or suggest all the elements of claim 9.

Araki teaches floating transitor gate having a three layered structure 104 upon a cell gate oxide 103, the cell gate oxide over a p-type silicon substrate 101. Fig. 4

represents this three layered structure by dashed lines and indicates a center portion, lower and upper portions. (See Fig. 4, Araki) The disclosure of Araki further defines this three layered structure by specifically reciting that "the first polysilicon layer 104 is formed so as to configure a three layered structure, such as a non-doped polysilicon/impurity doped polysilicon/non-doped polysilicon while changing the deposition condition." (Araki, column 3, lines 20-25).

Araki goes on to teach the importance of these non-doped layers in the fabrication of this floating gate. At column 4, lines 10-15, Araki teaches the importance of having an oxidized polysilicon surface with a low impurity density during low temperature oxidation to form the lower layer of the ONO intermediate layer. (Araki, column 4, lines 10-15) Araki specifically teaches the importance of having no impurity (phosphorous) in the lowest layer of polysilicon touching the cell gate oxide film. (Araki, column 4, lines 45-50)

Cl-72 ↓ poly has impurities

Araki is understood to teach a structure having a core of impurity doped polysilicon bordered on its upper side by a non-doped polysilicon having very little impurity, but most specifically bordered on its lower side by a non-doped polysilicon that does not contain any impurity. Araki discloses the necessity of a non-doped polysilicon lower side during the oxidation process to avoid damage to the cell gate oxide film with which the layer is in contact. In sum, Araki specifically teaches a floating gate transistor having non-doped polysilicon portion (104) upon, and in contact with a cell gate oxide (103).

Claim 9 is allowable for at least the reason that it recites forming; an oxide layer, a first layer of conductively doped semiconductive material upon and contacting the

oxide layer, and a second layer of substantially undoped semiconductive material over the first layer. Araki does not teach this limitation. Araki instead teaches the formation of an undoped layer in contact with the oxide layer of a floating gate transistor. Furthermore, Araki cannot be construed to teach or suggest the recited elements of claim 9 because Araki specifically teaches against the formation of an doped layer in contact with an oxide layer of a floating gate transistor.

Amended claim 9 is therefore allowable for at least the reason that it recites limitations not shown or suggested in the art. Applicant requests allowance of claim 9 in the Examiner's next action.

Claims 10-14 all depend from claim 9 and therefore are allowable for at least the reasons cited above regarding claim 9.

Claim 25 has been amended and as amended recites, in pertinent part, the formation a first oxide-containing layer over a substrate, forming a first layer comprising polysilicon upon the first oxide-containing layer, and the first layer comprising polysilicon being in contact with the first oxide-containing layer. Claim 25 further recites doping the first layer comprising polysilicon to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq. In sum, claim 25 recites, in pertinent part, a doped first layer comprising polysilicon in contact with a first oxide-containing layer formed over a substrate. As discussed above, the cited reference does not teach or suggest this limitation. Applicant requests allowance of claim 25 in the Examiner's next action.

Claims 26-31 all depend from claim 25 and are therefore allowable for at least the reasons cited above regarding claim 25.

New claims 72-77 have been added and are supported by the specification at, for example, pages 4 and 5 and Figures 7 and 8. No new matter has been added.

New claim 72 recites, in pertinent part, a silicon-containing material having a first region in direct physical contact with the oxide-containing layer and a second region spaced form the oxide-containing layer by the first region. Claim 72 further recites the first region having a higher concentration of conductivity enhancing impurity than any conductivity enhancing impurity in the second region. For at least the reason that claim 72 recites a first region in direct physical contact with the oxide-containing layer and the first region having a concentration of conductivity enhancing impurity, and the cited references do not teach or suggest this limitation, claim 72 is allowable. Action to that end is earnestly solicited.

Claims 73-77 depend from claim 72 and are therefore allowable for at least the reasons discussed above regarding claim 72.

Having addressed all of the issues raised by the Examiner in the last Action, and proffered the patentability of additional claims, this application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

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